REMARKS

The present amendment is in response to the Office Action mailed December 31, 2002, in which Claims 1 through 20 were rejected. Applicant has thoroughly reviewed the outstanding Office Action including the Examiner's remarks and the reference cited therein. The following remarks are believed to be fully responsive to the Office Action and, when coupled with the amendments made herein, are believed to render all claims at issue patentably distinguishable over the cited references.

Claims 6, 8 and 16 are amended herein. Claims 1 through 5, 7 and 11 through 15 are cancelled. No claims are added. Accordingly, Claims 6, 8 through 10, and 16 through 20 remain pending.

All the changes are made for clarification and are based on the application and drawings as originally filed. It is respectfully submitted that no new matter is added.

Applicant respectfully requests reconsideration in light of the above amendments and the following remarks.

CLAIM REJECTIONS – 35 U.S.C. SECTION 103(a)

1. Claims 1 and 5

With respect to Paragraph 2 of the final Office Action, the Examiner rejected Claims 1 and 5 under 35 U.S.C. Section 103(a) as being unpatentable

over U.S. Patent No. 5,933,733 to Feria *et al.* (hereinafter referred to as "Feria *et al.*") in view of U.S. Patent No. 5,972,783 to Arai *et al.* (hereinafter referred to as "Arai *et al.*"). Of the rejected claims, Claim 1 is independent.

Applicant respectfully traverses these rejections on the ground that they are moot in view of the fact that Claims 1 and 5 are cancelled herein.

Reconsideration and withdrawal of the rejection of Claims 1 and 5 under 35 U.S.C. Section 103(a) are respectfully requested.

2. Claims 2, 3 and 4

With respect to Paragraph 3 of the final Office Action, the Examiner rejected Claims 2, 3 and 4 under 35 U.S.C. Section 103(a) as being unpatentable over Feria *et al.* in view of Arai *et al.* and in further view of US Patent No. 4,937,756 to Hsu *et al.* (hereinafter referred to as "Hsu *et al.*").

Applicant respectfully traverses these rejections on the ground that they are moot in view of the fact that Claims 2, 3 and 4 are cancelled herein.

Reconsideration and withdrawal of the rejection of Claims 2, 3 and 4 under 35 U.S.C. Section 103(a) are respectfully requested.

3. Claims 6, 9, 10, 11, 14 and 15

With respect to Paragraph 4 of the final Office Action, the Examiner rejected Claims 6, 9, 10, 11, 14 and 15 under 35 U.S.C. Section 103(a) as

being unpatentable over Feria *et al.* in view of Arai *et al.* and in further view of US Patent No. 6,030,871 to Eitan *et al.* (hereinafter referred to as "Eitan *et al.*"). Of the rejected claims, only Claims 6 and 11 are independent.

Applicant respectfully traverses this rejection.

Claims 7 and 11 through 15 are deleted. Claims 6 and 8 are amended. Amended Claim 6 recites forming a stacked oxide-nitride-oxide layer on a P-type semiconductor substrate, patterning the stacked oxide-nitride-oxide layer to form a plurality of nitride read only memory cells on the P-type semiconductor substrate, and forming a plurality of indium pocket regions in the P-type semiconductor substrate under the gate structure of each of the nitride read only memory cells, and afterward, performing an N-type ion implantation to form a plurality of N-type ion-implanted regions in the P-type semiconductor substrate beside each of the indium pocket regions.

With regard to Feria *et al.*, this reference teaches a process to form memory cells wherein a P-type semiconductor substrate is provided (see col. 8, lines 15 through 25), and a dielectric layer is formed thereon (see FIG. 2). On the dielectric layer a photoresistor layer is formed and patterned to expose a portion of the dielectric layer (see FIG. 3). The dielectric layer is then etched using the photoresistor layer as a mask (see FIG. 3). Then, an N-type ion implantation is performed to form a plurality of N-type ion-implanting regions in the P-type semiconductor substrate so as to form source/drain regions (see

FIG. 4). Afterward, an ion implantation is performed to form a plurality of pocket dopant regions, each of which is disposed beside one of source/drain regions (see FIGs. 5 and 6).

With regard to Arai *et al.,* this reference teaches a process for producing MOS transistors wherein an ion implantation step to form pockets includes the implantation of indium (see col. 20, lines 15 through 20).

With regard to Eitan *et al.*, this reference teaches the formation of memory cells, wherein a sacrificial oxide layer is formed on the semiconductor substrate, then a first ion implantation is performed to form source/drain regions and a second ion implantation is performed to form pocket dopant regions (see FIGs. 4A, 4B and 4C).

As claimed in amended Claim 6, the stacked oxide-nitride-oxide is formed on the P-type semiconductor substrate prior to the formation of the indium pocket regions and the source/drain regions, which can prevent undesired diffusion of the implanted dopants caused by later thermal steps of forming the gate insulating layer of stacked oxide-nitride-oxide. However, all of the three cited references, Feria *et al.,* Arai *et al.* and Eitan *et al.*, when standing alone or in combination, fail to teach or suggest forming a stacked oxide-nitride-oxide layer on the semiconductor substrate before the ion implantation steps. Thus, it is not obvious for one-skilled in the art to deduce amended Claim 6 in view of Feria *et al.,* Arai *et al.* and Eitan *et al.* Amended

Claim 6 is patentably distinguishable over the three cited references.

Amended Claims 8, 9 and 10 depend upon independent Claim 6, each of which include all of the limitations thereof. Thus, amended Claim 8, 9 and 10 are also patentably distinguishable over the three cited references.

Applicant respectfully requests that the Examiner's 35 U.S.C. Section 103(a) rejection of Claims 6, 9, 10, 11, 14 and 15 be reconsidered and withdrawn.

4. Claims 7, 8, 12, 13, and 16 through 20

With respect to Paragraph 5 of the final Office Action, the Examiner rejected Claims 7, 8, 12, 13 and 16 through 20 under 35 U.S.C. Section 103(a) as being unpatentable over Feria *et al.* in view of Arai *et al.* and Eitan *et al.* and in further view of Hsu *et al.* Of the rejected claims only Claim 16 is independent.

Applicant respectfully traverses this rejection.

Amended Claim 16 recites forming a stacked oxide-nitride-oxide layer on a P-type semiconductor substrate, patterning the stacked oxide-nitride-oxide layer to form a plurality of nitride read only memory cells on the P-type semiconductor substrate, and performing an N-type ion implantation to form a plurality of N-type ion-implanted regions in the P-type semiconductor substrate to form source/drain regions, then forming a plurality of indium pocket regions

in the P-type semiconductor substrate, each of which beside one of the source/drain regions.

With regard to Hsu *et al.,* the Examiner's attention is respectfully directed to col. 3, lines 30 through 45 and FIG. 4-4, which teach that a certain amount of boron is implanted into the isolation region as shown by reference numeral 4 before the GIS is defined. A composite thermal oxide-nitride-oxide structure is then formed on the P-type semiconductor substrate as the GIS gate insulator 5.

It is apparent that Hsu *et al.* fail to teach or suggest forming a stacked oxide-nitride-oxide layer on the semiconductor substrate before the ion implantation step. Thus, it is not obvious for one-skilled in the art to deduce amended Claim 16 in view of Feria *et al.,* Arai *et al.,* Eitan *et al.* and Hsu *et al.*, when taken alone or in combination. Applicant respectfully submits that amended Claim 16 is patentably distinguishable over the four cited references.

Claims 17 through 20 depend upon Claim 16, each of which include all of the limitations thereof. Thus, Claims 17 through 20 are also distinguishable over the four cited references.

Amended Claim 8 is also patentably distinguishable over the four cited references based on the same reason.

Applicant respectfully requests that the Examiner's 35 U.S.C. Section 103(a) rejection of Claims 7, 8, 12, 13 and 16 through 20 be reconsidered and

withdrawn.

MARKED-UP CHANGES

Attached hereto is a marked-up version of the changes made to the claims by the current amendment. The attached paper is captioned **"VERSION WITH MARKINGS TO SHOW CHANGES MADE."**

ENTRY OF AMENDMENT AFTER FINAL

It is respectfully submitted that the present amendment should be entered in accordance with the provisions of 37 C.F.R. Section 1.116 on the grounds that: (1) The claims as now presented are in better form for appeal purposes, if necessary; (2) no new issues have been raised; (3) and, moreover, the present amendment is believed to place the application in condition for allowance.

CONCLUSION

In light of the above amendments and remarks, Applicant respectfully submits that all pending Claims 6, 8 through 10, and 16 through 20 as currently presented are in condition for allowance. If, for any reason, the Examiner disagrees, please call the undersigned attorney at 202-624-3947 in an effort to resolve any matter still outstanding *before* issuing another action.

The undersigned attorney is confident that any issue which might remain can readily be worked out by telephone.

Applicant respectfully requests that a timely Notice of Allowance be issued in this case.

Respectfully submitted,

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Dated: **March 31, 2003**

TTM/hs

VERSION WITH MARKINGS TO SHOW CHANGES MADE
(USSN 09/870,530)

IN THE CLAIMS:

Claims 1 through 5, 7 and 11 through 15 have been cancelled.

Claims 6, 8 and 16 have been amended as follows:

6. (Amended) A method for forming a nitride read only memory, the method comprising:

providing a P-type semiconductor substrate;

forming a stacked oxide-nitride-oxide [dielectric] layer on said P-type semiconductor substrate;

forming and defining a plurality of photoresister layers on said stacked oxide-nitride-oxide [dielectric] layer to expose a portion of said stacked oxide-nitride-oxide [dielectric] layer;

performing an etching process by way of using said plurality of photoresister layers as a plurality of etching masks to etch said stacked oxide-nitride-oxide layer and form a plurality of read only memory cells;

performing a pocketed ion-implantation with an indium ion at least one time by way of using said plurality of photoresister layers as a plurality of ion-implanting masks to form a plurality of pocket dopant regions having said indium ion in said P-type semiconductor substrate;

[and]

performing afterward an [a] N-type ion-implanting process by way of using said plurality of photoresister layers as said ion-implanting masks to form a plurality of N-type ion-implanting regions in said P-type semiconductor substrate between said plurality of photoresist layers; and

removing said plurality of photoresist layers to form said read only memory.

8. (Amended) The method according to claim 6, wherein the method for forming said stacked oxide-nitride-oxide [dielectric] layer comprises a depositing process.

16. (Amended) A method for forming a [an] nitride read only memory, the method comprising:

providing a P-type semiconductor substrate;

forming an oxide-nitride-oxide layer on said P-type semiconductor substrate;

forming and defining a plurality of photoresister layers on said oxide-nitride-oxide layer to expose a portion of said oxide-nitride-oxide layer;

performing an etching process by way of using said plurality of photoresister layers as a plurality of etching masks to etch said oxide-nitride-

oxide layer and form a plurality of read only memory cells;

performing an [a] N-type ion-implanting process by way of using said plurality of photoresister layers as an ion-implanting masks to form a plurality of N-type ion-implanting regions in said P-type semiconductor substrate between said plurality of read only memory cells;

performing a pocketed ion-implantation with an indium ion at least two time by way of using said plurality of photoresister layers as said plurality of ion-implanting masks to form a plurality of pocket dopant regions having said indium ion beside said P-type semiconductor substrate under said plurality of memory cells; and

removing said plurality of photoresist layers to form said nitride read only memory.